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(71) Applicant:
STMicroelectronics S.r.l.
20041 Agrate Brianza (Milano) (IT)

(72) Inventors:
- **Patelmo, Matteo**
  20044 Bernareggio (IT)
- **Vajana, Bruno**
  24100 Bergamo (IT)
- **Dalla Libera, Giovanna**
  20052 Monza (IT)
- **Cremonesi, Carlo**
  20069 Vaprio d'Adda (IT)
- **Galbiati, Nadia**
  20038 Seregno (IT)

(74) Representative:
Cerbaro, Elena, Dr. et al
STUDIO TORTA S.r.l.,
Via Viotti, 9
10121 Torino (IT)

(54) Method for manufacturing EEPROM with periphery

(57) The step of forming source and drain regions (48', 55') for LV transistors includes the steps of forming sacrificial spacers (101) laterally to LV gate regions (43a); forming LV source and drain regions (55') in a self-aligned manner with the sacrificial spacers (101); removing the sacrificial spacers (101); forming HV gate regions (43d) of HV transistors; forming gate regions (43c) of selection transistors; forming control gate regions (43b) of memory transistors; simultaneously forming LDD regions (48') self-aligned with the LV gate regions (43a), HV source and drain regions (64) self-aligned with the HV gate regions (43d), source and drain regions (65a, 65b) self-aligned with the selection gate region (43c) and floating gate region (27b); depositing a dielectric layer; covering the HV and memory areas with a protection silicide mask (72); anisotropically etching the dielectric layer, to form permanent spacers (52') laterally to the LV gate regions (43a); removing the protection silicide mask (72); and forming silicide regions (75a1, 75a2) on the LV source and drain regions (48', 55') and on the LV gate regions (43a).

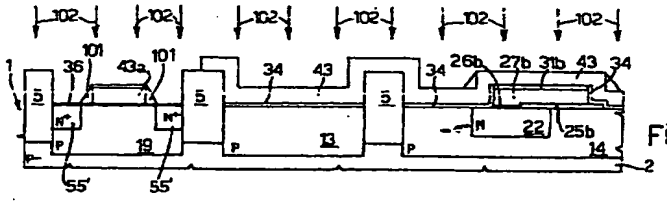

Fig.26

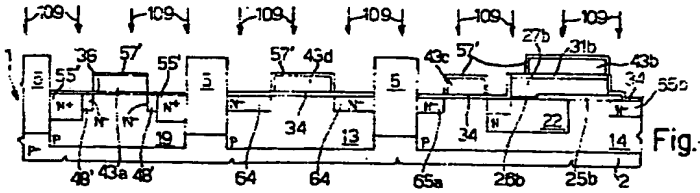

Fig.29

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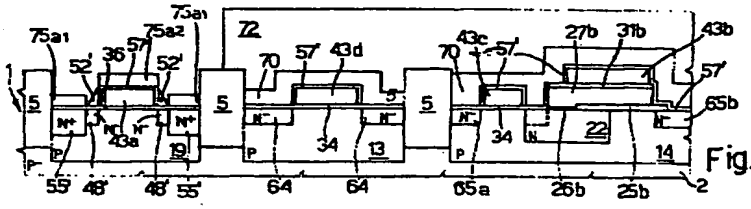

75a1
75a2
75a1
Z2
52'
36'
57'
52'
70
57'
43d
70
43c
57'
27b
31b
43b
57'
65b
5
5
5
5
N+
N+
N-
N-
N-
N-
N-
43a
19'
34
13
34
22
14
P
P
P
P
55'
48'
48'
55'
64
64
65a
26b
25b
2

Fig.30

Description

[0001] The present invention relates to a method for manufacturing electronic devices, comprising non-salicided non-volatile memory cells, non-salicided HV transistors, and LV transistors with salicided junctions.

[0002] The need has recently arisen in advanced processes (gate lengths of 0.35 μm or less), to integrate non-volatile memories of REPROM type in high-speed devices that use the technique of saliciding of the diffusions. As known, this technique is based on the use of a self-aligned silicide layer (salicide), which reduces the resistivity of the junctions. The salicide layer (typically made of titanium, but also of cobalt or another transition metal) is produced by depositing a titanium layer on the entire surface of the device, and carrying out a heat treatment which makes the titanium react with the silicon, left bare on the junctions and the gate regions, such as to form titanium silicide. Subsequently, the non-reacted titanium (for example deposited on oxide regions) is removed by etching using a suitable solution, which leaves the titanium silicide intact. Thereby, both the gate regions and the junctions have a parallel silicide layer with low resistivity (approximately 3-4 Ω/square), which reduces the resistance in series to the transistors. The salicide technique is described for example in the article "Application of the self-aligned titanium silicide process to very large-scale integrated n-metal-oxide-semi-conductor and complementary metal-oxide-semiconductor technologies", by R.A. Haken, in J. Vac. Sci. Technol. B, vol. 3, No. 6, Nov/Dec 1985.

[0003] The high voltages necessary for programming non-volatile memories (higher than 16 V) are however incompatible with saliciding the diffusions of memory cells, since the breakdown voltage of salicided junctions is lower than 13 V.

[0004] Process flows are therefore studied allowing integration of non-volatile memory cells and high-speed transistors with saliciding; however, this integration is made difficult by the fact that these components have different characteristics, and require different process steps. The large number of necessary masks is also disadvantageous in these flows.

[0005] The object of the present invention is thus to provide a manufacturing method with fewer masks than known methods, simple and with the lowest possible costs.

[0006] According to the present invention, a method is provided for manufacturing electronic devices, comprising non-volatile memory cells, HV transistors and LV transistors, as defined in claim 1.

[0007] To help understanding of the present invention, a preferred embodiment is now described, purely by way of non-limiting example, with reference to the attached drawings, in which:

- figure 1 shows a cross-section of a silicon wafer in a first step of a known production method;
- figure 2 is a plan view of the wafer of figure 1;
- figures 3-7 show cross-sections similar to that of figure 1, in successive production steps;
- figure 8 is a plan view of the wafer of figure 7;
- figures 9-11 show cross-sections similar to that of figure 7, in successive production steps;
- figure 12 is a plan view of the wafer of figure 11;
- figures 13-17 show cross-sections similar to that of figure 11, in successive production steps;
- figure 18 is a plan view of the wafer of figure 17;
- figures 19-21 show cross-sections similar to that of figure 17, in successive production steps;
- figure 22 is a plan view of the wafer of figure 21;
- figures 23-25 show cross-sections similar to that of figure 21, in successive production steps;
- figure 26 shows a cross-section through a silicon wafer, in a step of the method according to the invention;
- figure 27 shows a cross-section similar to that of figure 26, in a successive production step of the method according to the invention;
- figure 28 is a plan view of the wafer of figure 27; and
- figures 29-30 show cross-sections similar to that of figure 27, in successive production steps of the method according to the invention.

[0008] To help understanding of the present invention, a production method subject of European patent application 98830644.5, filed on 23.10.1998 in the name of the same applicant, is initially described with reference to figures 1 to 25. In detail, this method makes it possible to produce a device comprising LV (low-voltage and high-speed) and HV (high-voltage) NMOS transistors, LV and HV PMOS transistors, and EEPROM memory cells formed by a selection transistor and a memory transistor.

[0009] In particular, owing to the duality in forming NMOS and PMOS transistors, the drawings show only the steps for NMOS transistors, and the steps for forming PMOS transistors are described in words alone. The EEPROM memory cells form a memory array, and are produced in a part of the wafer thereafter also designed matrix area 15.

[0010] In figure 1, a wafer 1 formed by a monocrystalline silicon substrate 2, here of P type, has been subjected, to the active area definition steps. In detail, with the surface 3 of the substrate 2 covered by an active area mask 4 of non-oxidisable material (typically of a double layer of silicon oxide and silicon nitride, defined using resist), wafer 1 has been subjected to thermal oxidation; consequently, in the parts of the substrate 2 not covered by the active area mask 4, thick oxide layers (field oxide 5) have been grown, delimiting between each other active areas of the substrate, designed to accommodate various components of the device to be produced. In particular, figure 1 shows three active areas, i.e. a LV active area 6, designed to accommodate

a LV NMOS transistor, an HV active area 7, designed to accommodate an HV NMOS transistor, and an active matrix area 8, designed to accommodate EEPROM memory cells.

[0011] In detail, and in a known manner, the active matrix area 8 defines a grid, of which figure 2 shows in full only the part relative to one cell, indicated at 9, having substantially the shape of a "T" rotated by 90°, and comprises a leg 9a and a cross-piece 9b. The leg 9a is adjacent to, and electrically connected to, respective legs 9a of other cells arranged above and below the shown cell, of which only parts are visible; in addition, the leg 9a is connected to a leg of an adjacent cell to the right (not shown), which has a symmetrical structure with respect to that shown. The legs 9a are designed to accommodate source regions of the memory transistors; the end of the cross-pieces 9b not connected to the legs 9a is designed to accommodate drain regions of the selection transistors, and the gate regions of the cells must be provided on the cross-pieces 9b. Further active areas are generally provided for forming LV or HV PMOS transistors, not shown in the drawings.

[0012] Subsequently, the active area mask 4 is removed, the free surface 3 of the substrate is oxidated to form a sacrificial oxide layer 10, and doping ions of N type are implanted through a mask, for forming N-HV regions (not shown) for the HV PMOS transistors; using an HV P-well resist mask 11, covering the entire surface of wafer 1, except active HV area 7 and matrix area 8, doping ions of P type are implanted, as shown schematically in figure 3 by arrows 12.

[0013] In the substrate 2, P-HV regions 13 of P type for high-voltage transistors, and a P-matrix region 14, also of P type, for the cells are then formed, as shown in figure 3. The P-HV regions 13 and P-matrix regions 14 reproduce exactly the shape of the active HV area 7 and matrix area 8, and thus, for each cell, legs 14a (corresponding to legs 9a of active cell areas 9, see figure 8), and cross-pieces 14b (figure 8, corresponding to cross-pieces 9b) are defined.

[0014] After removing the HV P-well mask 11, doping ions of N type are implanted through a mask for forming N-LV regions (not shown) for the LV PMOS transistors; then, using a LV P-well resist mask 17 covering the entire surface of the wafer 1, except active LV areas 6, doping ions of P type are implanted, as shown schematically in figure 4, by arrows 18. In the substrate 2, P-LV regions 19 of P type for the LV NMOS transistors are then formed, as shown in figure 4. Thereby, the P-HV region 13 and the P-LV regions 19 are separated from one another, and their electrical characteristics can be optimised with respect to the electrical characteristics required.

[0015] After removing the LV P-well mask 17, a capacitor mask 20 is produced, covering the entire surface of wafer 1, except strip, perpendicular to cross-pieces 14b. Doping ions of N type (for example phosphorous) are then implanted, as shown schematically in figure 5 by arrows 21. In the cross-pieces 14b, continuity regions 22, of N type, are then formed, as necessary for electrical continuity between each selection transistor and the respective memory transistor of each cell. The structure of figure 5 is then obtained.

[0016] After removing the capacitor mask 20, the wafer 1 is subjected to annealing, the sacrificial layer 10 is removed, and matrix oxidation is carried out, forming a matrix oxide layer 25 on the surface of all regions 13, 14, and 19. Then, using a matrix oxide mask 24, shown in cross-section in figure 7 and in plan view in figure 8, the matrix oxide is removed from everywhere except from beneath the matrix oxide mask 24, forming a region 25b in the P-matrix region 14 that is partially arranged above the continuity region 22, and partially covers the leg 9a, and a masking region 25a on the P-LV region 19 (figure 7).

[0017] After removing the matrix oxide ask 24, wafer 1 is oxidised again, forming a tunnel oxide layer 26 on the entire surface of the substrate, where the latter is exposed, and increasing the thickness of the oxide that is already present (regions 25a, 25b) in regions 14 and 19. The structure of figure 9 is thus obtained.

[0018] A first polycrystalline silicon layer is then deposited (polyl layer 27), which is suitably doped; subsequently, an interpoly dielectric layer 31 is formed, for example of a triple layer of ONO (silicon oxide-silicon nitride-silicon oxide), as shown in figure 10.

[0019] A floating gate mask 30 shown in figure 11 and 12 is then formed; dielectric layer 31, polyl layer 27, and tunnel oxide layer 26 are then etched everywhere except where the floating gate regions of the memory transistors are to be formed, indicated at 27b in figure 11; consequently, of the tunnel oxide layer 26, only a tunnel region 26b is left, adjacent to an edge of the floating gate region 27b of the memory transistor. In this step, the thickness of the region 25a decreases again on the active area 19.

[0020] After removing the floating gate mask 30, an HV oxidation step is carried out, forming an HV gate oxide layer 34 on the entire free surface of substrate 2, in particular on P-HV regions 13 and P-matrix regions 14 (figure 13). Portions of oxide 34 are also formed laterally to the floating gate region 27b of the memory transistor, as shown in figure 13, and the thickness of the region 25a increases again. Subsequently, using an HV oxide resist mask 35, which covers the P-HV region 13 and the matrix area 15, the region 25a is removed from above the P-LV regions 19 (figure 14).

[0021] After removing the HV oxide mask 35, a LV oxidation step is carried out, forming a LV gate oxide layer 36 above the P-LV regions 19; in addition, the thickness of the HV gate oxide layer 34 increases above the P-HV region 13 and the P-matrix regions 14, thus providing the structure of figure 15.

[0022] Then a second polycrystalline layer (non-doped poly2 layer 43) is deposited, as shown in figure 16. A LV gate mask 44 is formed, covering the N-HV

regions (not shown), the P-HV regions 13, and the matrix area 15. In addition, the LV gate mask 44 covers the poly2 layer, above the P-LV regions 19, where both the NMOS and PMOS gate regions of the LV transistors must be defined, as shown in figures 17 and 18, and above the N-LV regions (not shown) where the gate regions of the LV PMOS transistors must be defined. The exposed portions of the poly2 layer 43 are removed, thus providing the structure of figure 17, wherein the portions of poly2 remaining above P-LV regions 19 form gate regions 43 of the LV NMOS transistors. As can be seen, during the step of defining the gate regions of the LV transistors, the layers above the P-HV regions 13 and P-matrix regions 14 are protected, as are the layers above the N-HV regions (not shown); consequently, the method described provides separate definition of the gate regions of the LV transistors and HV transistors, as well as of the memory cells.

[0023] After removing the LV gate mask 44, and re-oxidation, to seal the gate regions 43a of the LV NMOS transistors, using a resist mask not shown, which covers the N-LV and N-HV regions, doping ions of N type are implanted (LDDN implanting), as schematised in figure 19 by arrows 47. Laterally on the gate regions 43a (inside the P-LV regions 19), LDD regions 48 of N type are then formed; in addition, the poly2 layer 43 is suitably doped.

[0024] After removing the resist mask, not shown, masked implanting of doping ions of P type is carried out; in particular, during this step, the P-HV 13 regions and P-LV 19 regions, as well as the matrix region 15, are covered, whereas in the N-LV regions, LDD regions of type P (not shown) are formed. On the entire surface of the wafer 1, a dielectric layer (for example TEOS - TetraEthylOrthoSilicate) is then deposited; then, in a known manner, the TEOS layer is subjected to anisotropic etching, therefore it is removed completely from the horizontal portions, and remains laterally to the gate regions 43a, where it forms spacers 52, and partially on the floating gate regions 27b, on the matrix area 15 (figure 20). On the other hand, spacers are not formed above the field oxide regions 5, owing to the bird's beak shape of the latter (in a known manner, not shown for simplicity); furthermore, spacers are not formed above the P-HV regions 13 and the respective N-HV regions, since the gate regions of the HV transistors are not yet defined.

[0025] Subsequently, using a resist mask not shown, which covers the N-LV and N-HV reions, doping ions of N type are implanted, as schematised in figure 20 by arrows 54. LV-NMOS source and drain regions 55 of type N+ are then formed in the P-LV regions 19, in a self-aligned manner with the spacers 52. The LV-NMOS source and drain regions 55 are more highly doped than the LDD regions 48. In addition, the poly2 layer 43 and the gate regions 43a are doped N type, whereas the areas where HV and LV PMOS transistors are to be produced are covered. The structure of figure 20 is thus obtained.

[0026] After removing the resist mask (not shown), a similar step of masked implanting doping ions of P type is carried out, for forming respective source and drain regions in the N-LV regions (in a not shown manner), and for doping P type the poly2 layer 43, above the N-LV and N-HV regions. In this step, the P-LV regions 19, P-HV regions 13, and P-matrix region 14, are completely covered.

[0027] Subsequently, an HV gate mask 56 is formed, which covers the surface of the wafer 1, with the exception of the active areas where the gate regions of the high-voltage transistors are to be formed (P-HV regions 13, in the case of HV NMOS), and the portions of the P-matrix region 14 designed to form the gate regions of the selection transistor, and the control gate regions of the memory transistors (in this respect see figures 21 and 22). Then, the portions of poly2 layer 43 not covered by the HV gate mask 56 are etched; the structure of figure 21 is thus obtained.

[0028] Subsequently, re-oxidation is carried out, forming an oxide layer 57 on the entire free surface of substrate 2, in particular laterally on the floating gate regions 27b and control regions 43b of the memory transistors, and laterally on the gate regions of the selection transistors, as shown in figure 23, wherein the gate region of the selection transistor is indicated at 43c, the gate region of the memory transistor is indicated at 43b, and the gate region of the HV NMOS transistor is indicated at 43d.

[0029] After removing the HV gate mask 56 and re-oxidation, an NHV mask, not shown, is formed, covering N-LV and N-HV regions (not shown). Using the NHV mask, doping ions of N type are implanted, as shown schematically in figure 23 by arrows 63. In P-HV regions 13, at both sides of HV gate regions 43d, HV-NMOS source and drain regions 64 of N type are then formed, less doped than LV-NMOS source and drain regions 55; simultaneously, in the P-matrix region 14, drain regions 65a of selection transistor are formed, on one side, in a self-aligned manner with the gate regions 43c of the selection transistors, and the source regions 65b of the memory transistor are formed on the side not facing the respective selection transistor, in a aligned manner with the gate region 43b of the memory transistors. In addition, the areas arranged between each selection transistor and the respective memory transistor are also implanted; however, this implanting generally takes place inside the continuity regions 22, more doped, and is therefore not shown (for this reason the respective area is represented with broken lines). However, in case of misalignments, this implanting guarantees electrical continuity. The HV-NMOS source and drain regions 64 of the HV selection transistor 65a, and the source regions 65b of the memory transistor (as well as the drain regions) have a lower doping level than the LV-NMOS source and drain regions 55, and thus have a higher breakdown voltage and higher resistivity.

[0030] After removing the NHV mask, the source and drain regions of the HV PMOS transistors (not shown) are similarly implanted using a mask.

[0031] Subsequently a protection dielectric layer 70, for example of TEOS or nitride, is deposited on the entire surface of the wafer 1. A salicide protection mask 72 shown in figure 24, is then formed, covering the surface of wafer 1, except the active areas where the low-voltage transistors are formed (P-LV regions 19, for the NMOS). Using the salicide protection mask 72, dielectric layer 70 is removed from above the P-LV regions 19 (figure 24). After removing the salicide protection mask 72, if zener diodes, low-doping precision resistors, and/or transistors of N and P type with non-salicided junctions are to be formed, a dielectric layer is deposited and defined using a suitable mask, in a not shown manner. Otherwise, the uncovered poly2 layer are immediately salicided. Saliciding, carried out in a known manner, as previously described, causes titanium silicide regions to form above the source and drain regions of the LV NMOS and PMOS transistors (silicide regions 75a1 above the LV-NMOS source and drain regions 55, and similar regions for the LV PMOS transistors), above the gate regions of the LV NMOS and PMOS transistors (silicide regions 75a2 above the gate regions 43a for the LV NMOS transistors, and similar regions for the LV PMOS transistors), as shown in figure 25.

[0032] After forming a protection dielectric layer 78, the final structure of figure 25 is obtained, showing an LV NMOS transistor 80, an HV NMOS transistor 81, and an EEPROM cell 82, formed by a selection transistor 83 and a memory transistor 84. The final steps follow, including forming contacts and electrical interconnection lines, deposition of a passivation layer, etc.

[0033] As already stated, the method previously described requires many masks. To eliminate this problem, according to the invention a new manufacturing method is proposed, of which only the steps different from the preceding method are described.

[0034] In detail, the manufacturing method now described comprises initial steps that are the same as those described with reference to figures 1-18, up to defining the gate regions of the LV transistors. Then, after re-oxidation for sealing the gate regions 43a of the LV NMOS transistors, sacrificial spacers 101 are formed; doping ions are heavy implanted, and subsequently, after removing the sacrificial spacers, light implanting is carried out (LDD implanting).

[0035] In particular, on the entire surface of wafer 1, a sacrificial layer is deposited (of polysilicon, but also of a dielectric material such as nitride or TEOS-TetraEthylOrthoSilicate); then, in a known manner, the sacrificial layer is subjected to anisotropic etching, to remove it completely from the horizontal portions, while remaining on the sides of the gate regions 43a, where it forms sacrificial spacers 101, and, partially, on the floating gate regions 27b, on the matrix area 15 (figure 26).

[0036] Subsequently, using a resist mask, not shown, covering the N-LV and N-HV regions, N type doping ions are implanted, as schematised in figure 26 by arrows 102. LV-NMOS source and drain regions 55' of N+ type are then formed in the P-LV regions 19, in a self-aligned manner with the sacrificial spacers 101. In addition, in this step, poly2 layer 43 is suitably doped. Similarly to the previous method, after removing the resist mask, not shown, P type doping ions are implanted through a mask; in particular, during this step, P-HV regions 13, P-LV regions 19 and matrix area 15 are covered, whereas LDD regions of P type (not shown) are formed in the N-LV regions.

[0037] Then, the sacrificial spacers 101 are removed, and, as shown in figure 27, and in plan view in figure 28, an HV gate mask 106 is formed. The HV gate mask 106 covers the surface of the wafer 1, except the active areas where gate regions of the high-voltage transistors (P-HV regions 13, in the case of the HV NMOS), portions of the P-matrix region 14, designed to form the gate regions of the selection transistor, and control gate regions of the memory transistors are to be formed. Similarly to the previous method, in this step gate regions 43b, 43c and 43d are formed.

[0038] After removing the HV gate mask 106, re-oxidation is carried out, forming an oxide layer 57' on the entire free surface of the substrate 2, in particular laterally to gate regions 43a, 43b, 43c and 43d.

[0039] Then, using a resist mask, not shown, covering the N-LV and N-HV regions, light implanting of N type doping ions' is carried out (LDDN implanting), as schematised by arrows 109 in figure 29. Laterally to the gate regions 43a (inside the P-LV regions 19), LDD regions 48' of N type are then formed, less doped than LV-NMOS source and drain regions 55'.

[0040] Simultaneously, similarly to the previous method, in P-HV regions 13, HV-NMOS source and drain regions 64, and in the P-matrix region 14, drain regions 65a of the selection transistor and source regions 65b of the memory transistor are formed.

[0041] After removing the resist mask, not shown, similar masked implanting of doping ions of P type is carried out; in particular, during this step, P-HV regions 13, P-LV regions 19, and matrix zone 15 are covered, while P type LDD regions (not shown) are formed in the N-LV regions. On the entire surface of the wafer 1, a thick dielectric layer (for example TEOS-TetraEthyl-OrthoSilicate) is then deposited, as can be seen in figure 30 (dielectric layer 70).

[0042] Subsequently, a salicide protection mask 72, shown in figure 30, is formed, covering the surface of the wafer 1, except the active areas, where the low-voltage transistors are present (P-LV regions 19, in the case of NMOS). Using the salicide protection mask 72, the uncovered portion of the TEOS layer 70 is anisotropically etched, forming spacers 52' laterally on the gate regions 43a (figure 30).

[0043] After removing the salicide protection mask 72, the uncovered poly2 layer is salicised. As previously

described, saliciding forms titanium silicide regions 75a1, 75a2 above the source, drain and gate regions of the LV NMOS and PMOS transistors.

[0044] After forming a protection dielectric layer 78, the structure of the device obtained is the same as that according to the method previously described, and shown in figure 25. The final steps follow, including forming contacts and electrical interconnection lines, depositing a passivation layer etc. Thus, in the final device, as in the previous method, the EEPROM cells 72 are not salicided, and have a high breakdown voltage. Furthermore, memory transistor 84 is completely non-self-aligned. On the other hand, selection transistor 83 is self-aligned on both sides. This ensures a shorter structure, even in case of misalignments of individual shaping steps.

[0045] LV (NMOS and PMOS) transistors have a high-speed LDD structure with a dual gate (gate region 43a doped with ions of the same type as source and drain regions 48, 55); with salicided source and drain regions 55 and gate regions 43a.

[0046] The HV (NMOS and PMOS) transistors have a dual gate and drain extension, and are not salicided.

[0047] The described method thus forms simultaneously LV, HV and memory components with very different characteristics, thus optimising the number of manufacturing steps. In particular, compared with the method described in the aforementioned patent application, it is possible to use fewer masks, since it is not necessary to carry out separate N- and P-implanting of HV and LV transistors, and thus the N /P-regions can be subjected to a smaller number of thermal treatments.

[0048] In addition, since LDD implanting for forming LDD regions 48' is carried out defining the gate region 43d of the HV transistors, re-oxidation of the gate region 43d, comprising a heat treatment at 900°C, is carried out before light implanting of the LV transistors, and therefore ensures better control of the junction depth. Finally, it is apparent that any modifications and variants can be made to the method described and illustrated here, all within the scope of the invention, as defined in the attached claims.

Claims

1. A method for manufacturing electronic devices, comprising LV transistors (80), HV transistors (81) and memory cells (82), comprising the steps of:

   a) forming LV oxide regions (36) above first areas (19) of a silicon substrate (2) where low-voltage transistors are to be formed, HV oxide regions (34) above second areas (14) of said substrate where high-voltage transistors are to be formed, selection oxide regions (34), tunnel oxide regions (26b), and matrix oxide regions (25b), above third areas (13) of said substrate where selection transistors (83) and memory transistors (84) of EEPROM cells are to be formed;

   b) forming floating gate regions (27b) above said tunnel oxide regions and said matrix oxide regions;

   c) forming insulating regions (31b) above said floating gate regions;

   d) forming LV gate regions (43a) above said LV gate oxide regions;

   e) forming first source and drain regions (48', 55') laterally to said LV gate regions (43a);

   f) forming silicide regions (75a1, 75a2) on said LV source and drain regions (48', 55') and on said LV gate regions (43a);

   g) forming semiconductor material regions (43) completely covering said second and third areas (13, 14); and

   h) forming HV gate regions (43d) above said HV oxide regions, selection gate regions (430) above said selection oxide regions, and control gate regions (43b) above said insulating regions,

   wherein said step e) of forming first source and drain regions (48', 55') laterally to said LV gate regions (43a) comprises the steps of:

   i) forming sacrificial spacers (101) laterally to said LV gate regions (43a);

   j) forming LV source and drain regions (55') in said first areas (19), in a is self-aligned manner with said sacrificial spacers (101), said LV source and drain regions having a first doping level;

   k) removing said sacrificial spacers (101); and

   l) forming LDD regions (48') laterally to said LV gate regions (43a), inside said first areas (19), in a self-aligned manner with said LV gate regions (43a), said LDD regions (48') having a second doping level lower than said first level.

2. A method according to claim 1, characterised in that said step i) of forming sacrificial spacers (101) comprises the steps of:

   ii) depositing a sacrificial layer;

   i2) subjecting said sacrificial layer to anisotropic etching.

3. A method according to claim 1 or claim 2, characterised in that said steps i)-l) are carried out in sequence.

4. A method according to any one of the preceding claims, characterised in that in said step h), said HV gate regions (43d), selection gate regions (43c), and control gate regions (43b), are formed simultaneously by shaping said semiconductor material regions (43).

5. A method according to claim 4, characterised in that said step h) is carried out before said step 1) of forming LDD regions.

6. A method according to claim 4 or claim 5, characterised in that said step h) is carried out after said step j).

7. A method according to claim 4 or claim 5, characterised in that said step h) is carried out after said step k).

8. A method according to any one of the preceding claims, characterised in that said step h) is carried out before said step 1), and that simultaneously with said step 1), the step is carried out of:

   m) forming source and drain regions (64, 65a, 65b) in said second and third areas (13, 14), in an aligned manner with said HV gate regions (43d), said selection gate regions (43c) and said floating gate regions (27b).

9. A method according to claim 8, characterised in that it comprises, in sequence, after said step m), and before said step f), the steps of:

   n) depositing a dielectric material layer on said first (19), second (13) and third areas (14);
   o) forming a protection salicide mask (72) on said second (13) and third areas (14); and
   p) anisotropically etching maid dielectric material layer on said first areas (19), forming spacers (52') laterally to said LV gate regions (43a).

10. A method according to claim 9, characterised by the step of removing said salicide protection mask (72) before said step f).

11. A method according to any one of the preceding claims, characterised in that, after said step h) and before said step l), a re-oxidation step is carried out.

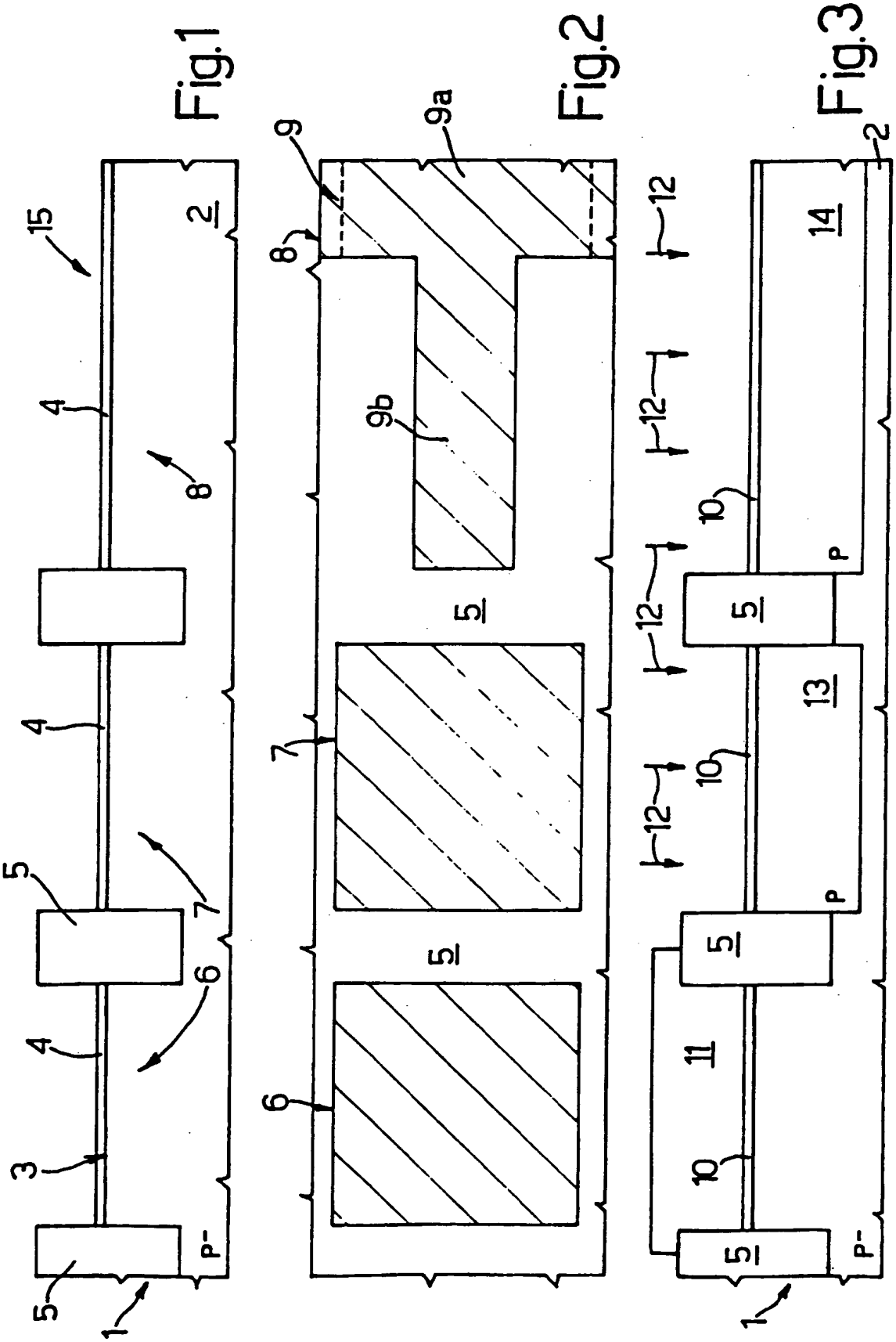
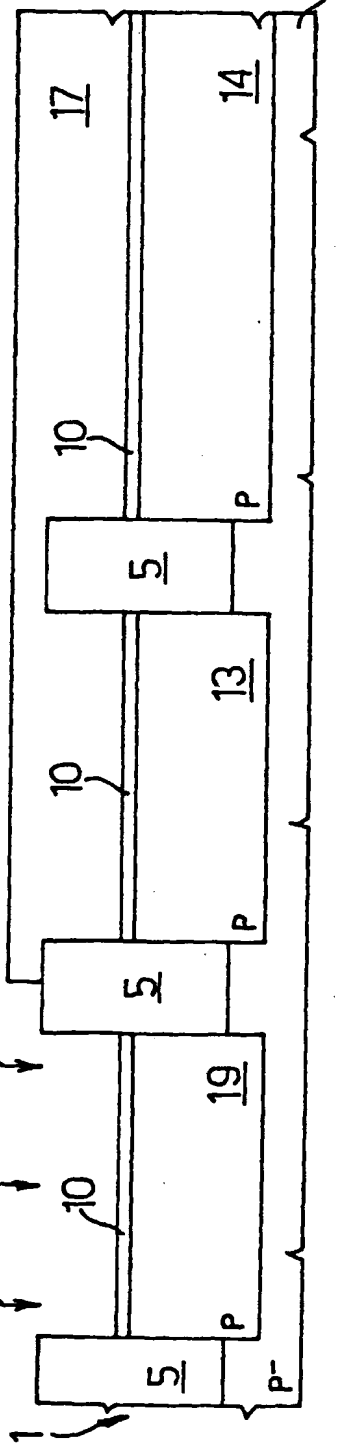


Fig.1
15
2
4
8
4
5
7
4
6
3
5
P-
1
Fig.2
9
9a
8
9b
5
7
5
6
Fig.3
12
14
2
12
10
12
5
P
13
12
10
5
P
11
5
10
5
P-
1

Fig.4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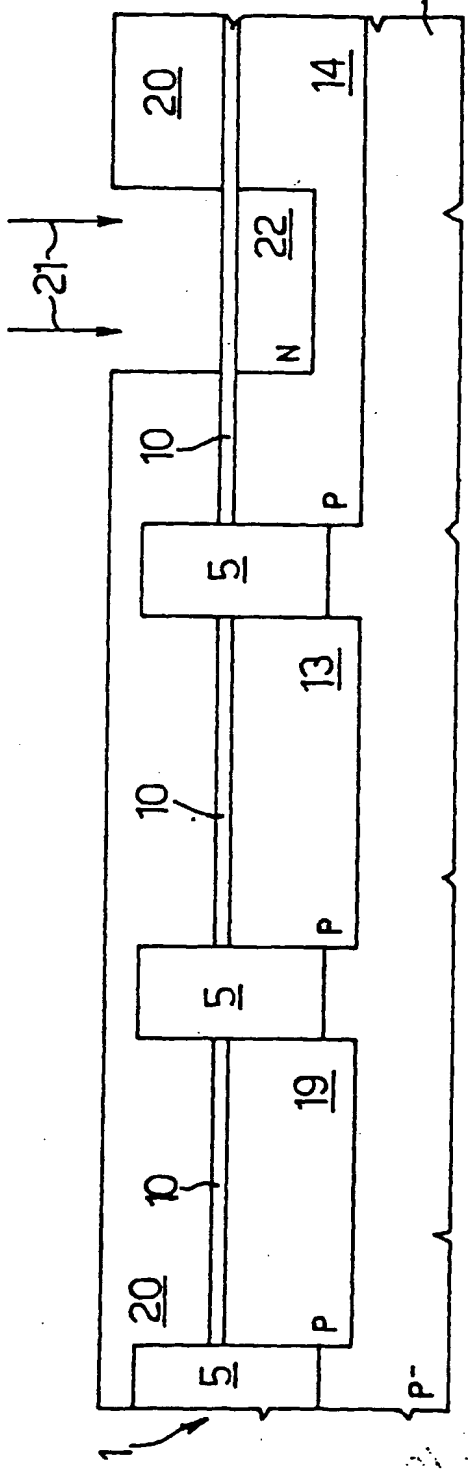
10
P
5
13
10
P
5
18
19
18
10
P
5
P-
1

Fig.5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22
21
N
10
P
5
13
10
P
5
19
10
20
P
5
P-
1

Fig.6

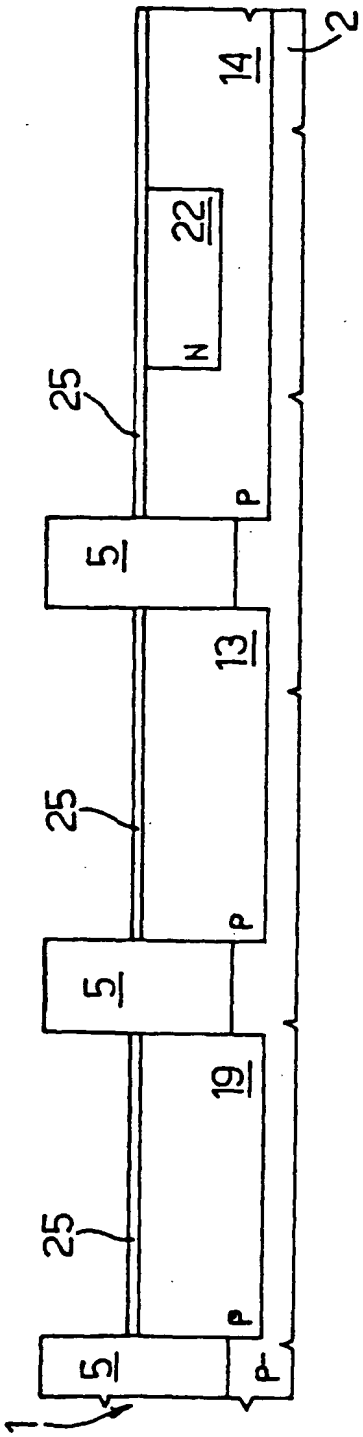


Fig.7

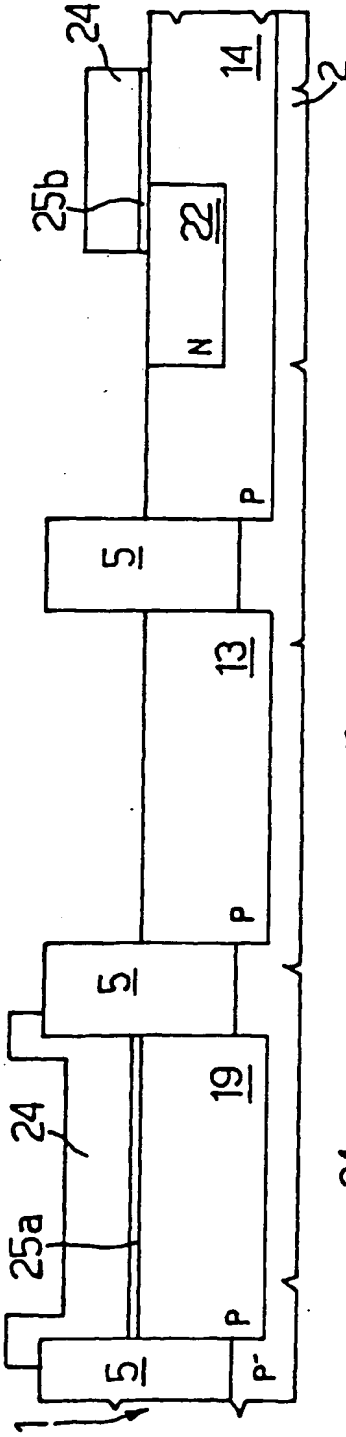


Fig.8

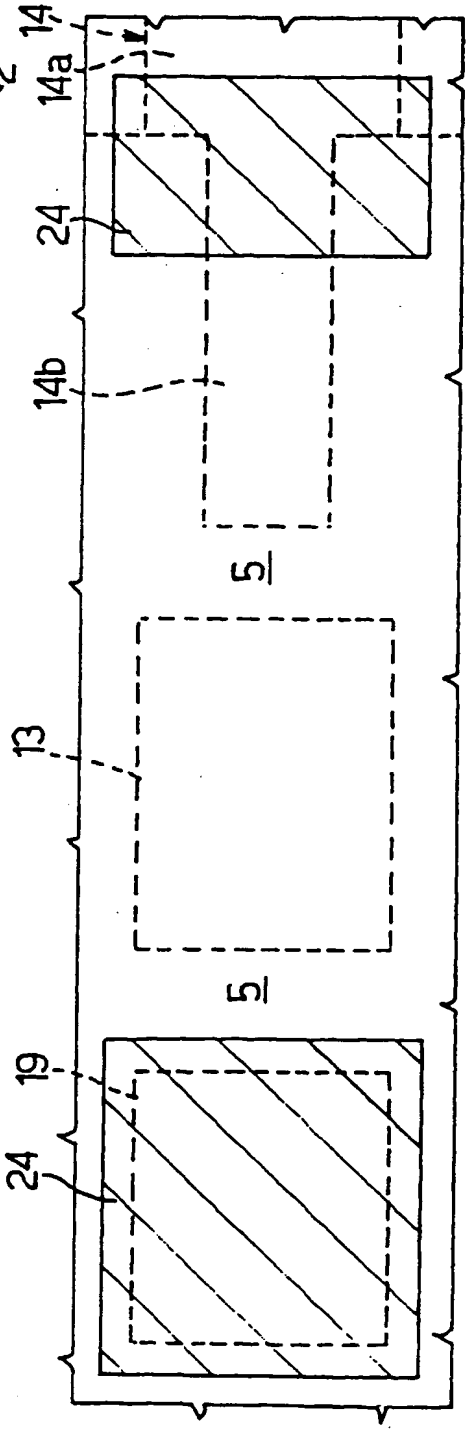
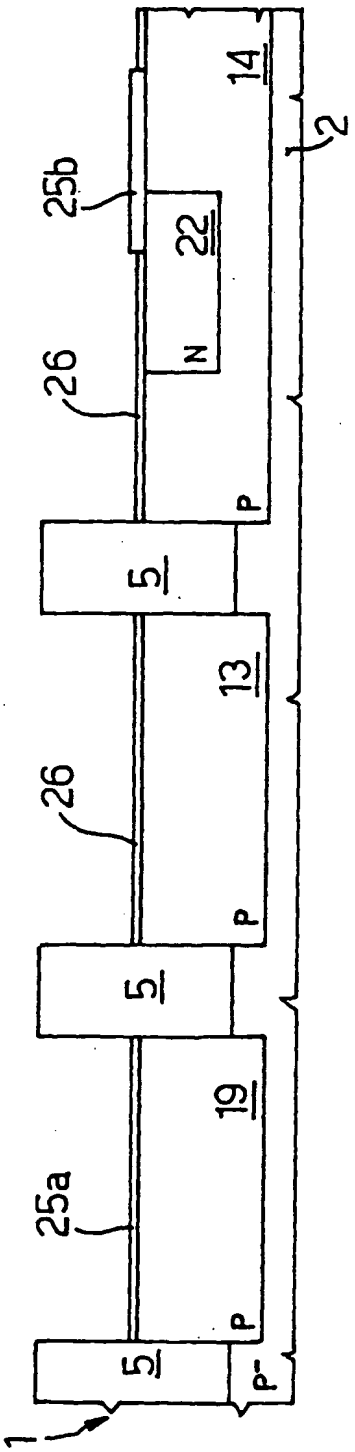


Fig.9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5
P-
P
25a
19
26
5
13
26
5
22
N
25b
14
2

Fig.10

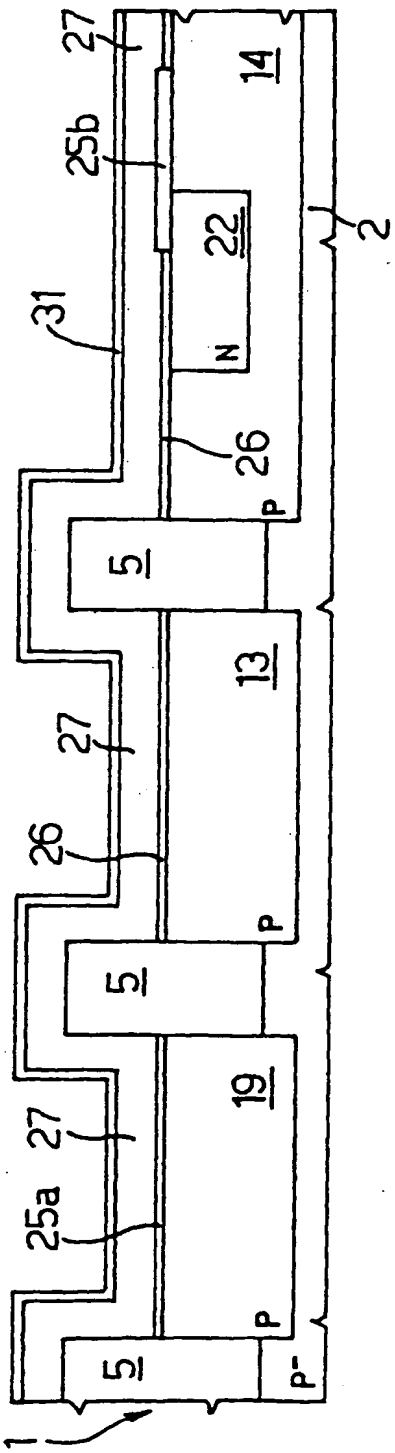

1
5
P-
P
25a
27
19
26
5
13
27
26
5
22
N
31
25b
27
14
2

Fig.11

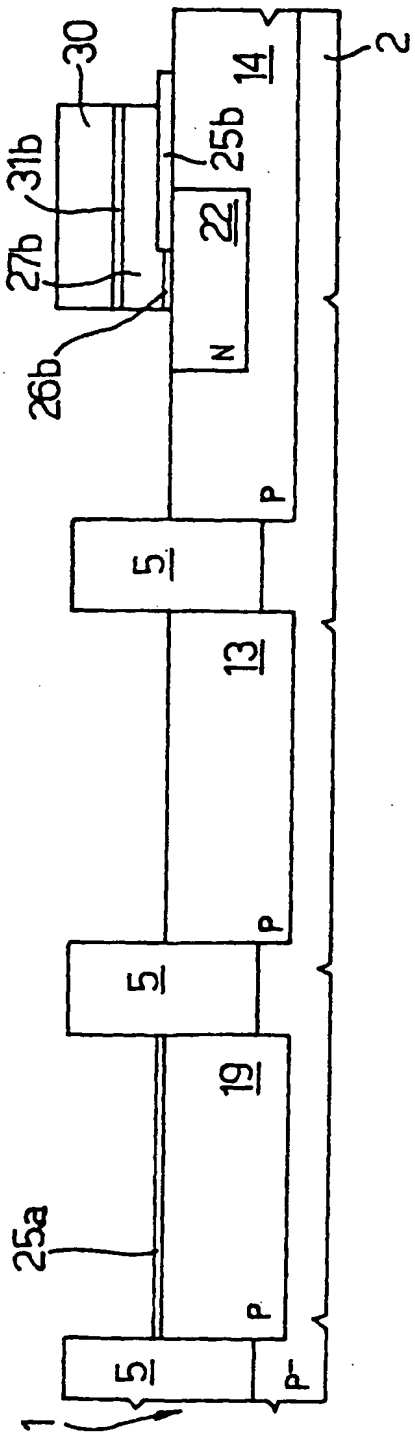


Fig.12

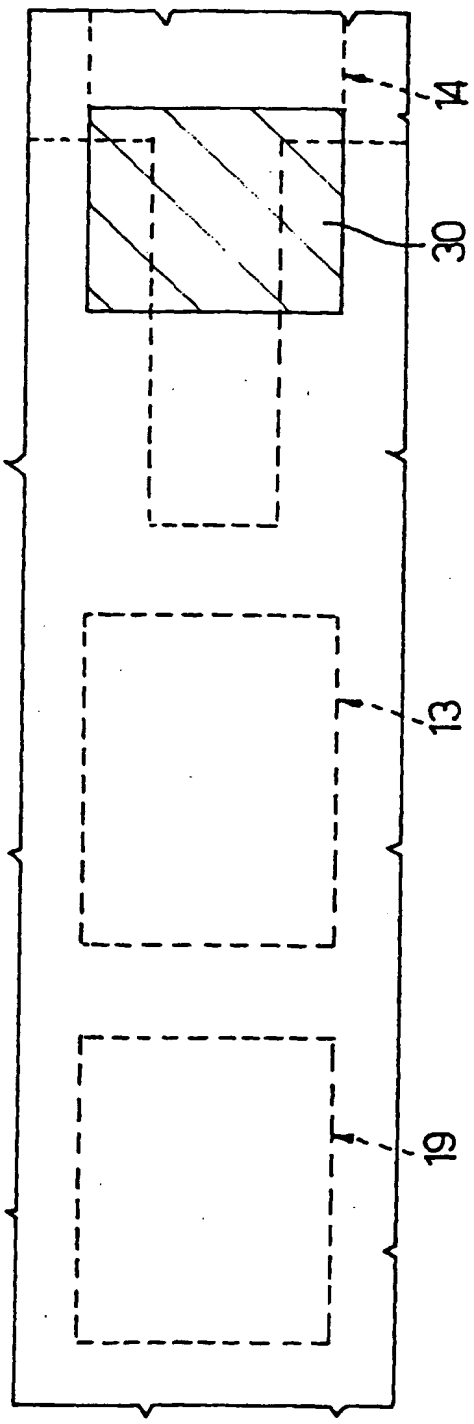


Fig.13

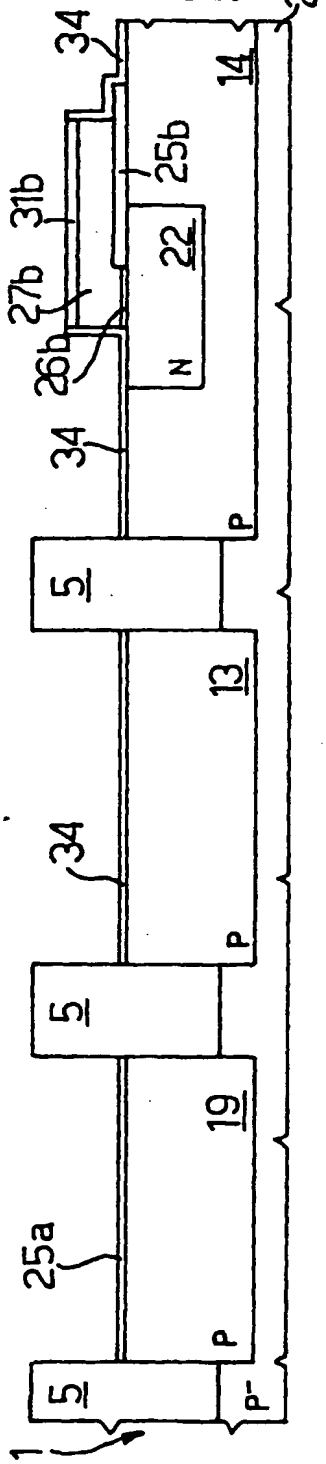


Fig.14

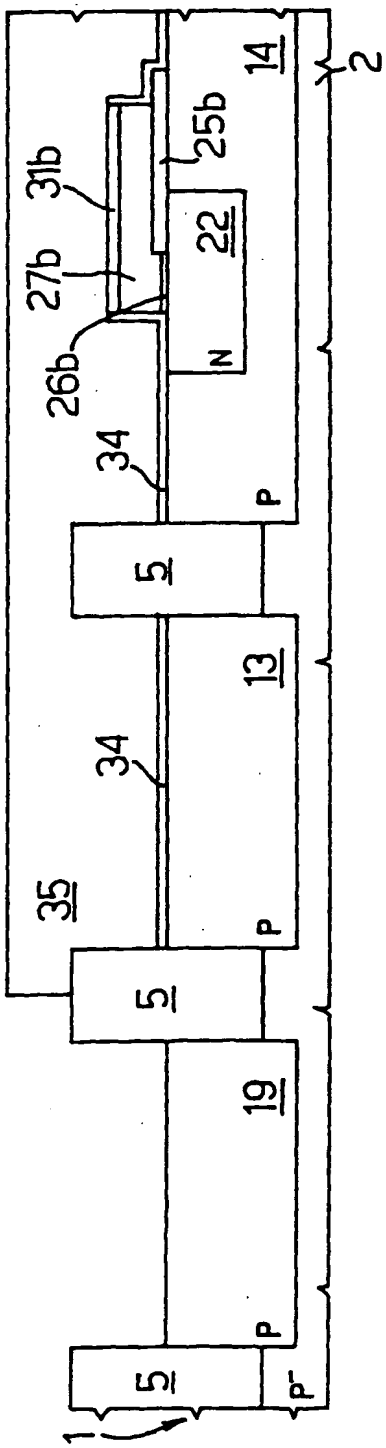


Fig.15

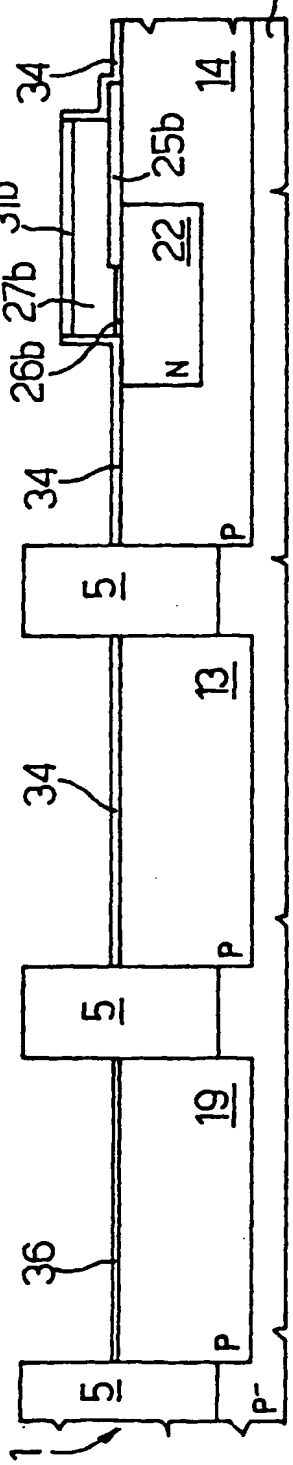


Fig.16

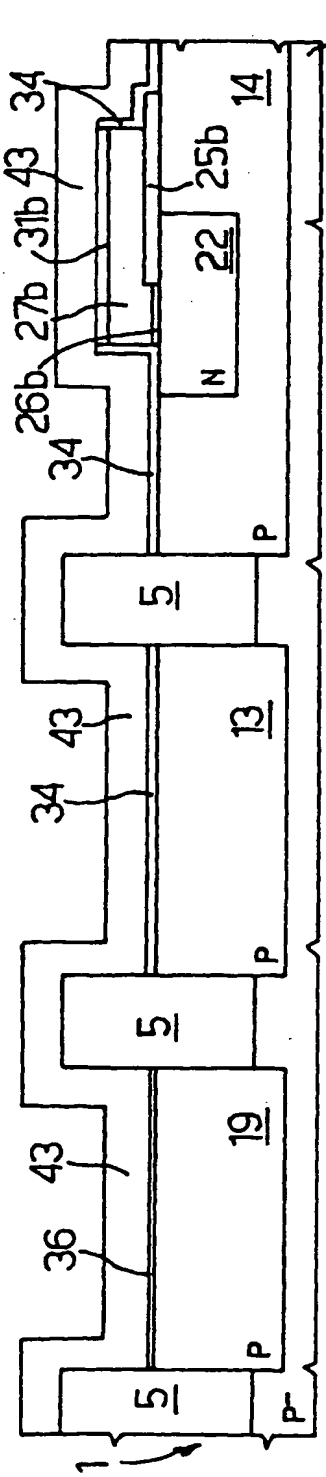


Fig.17

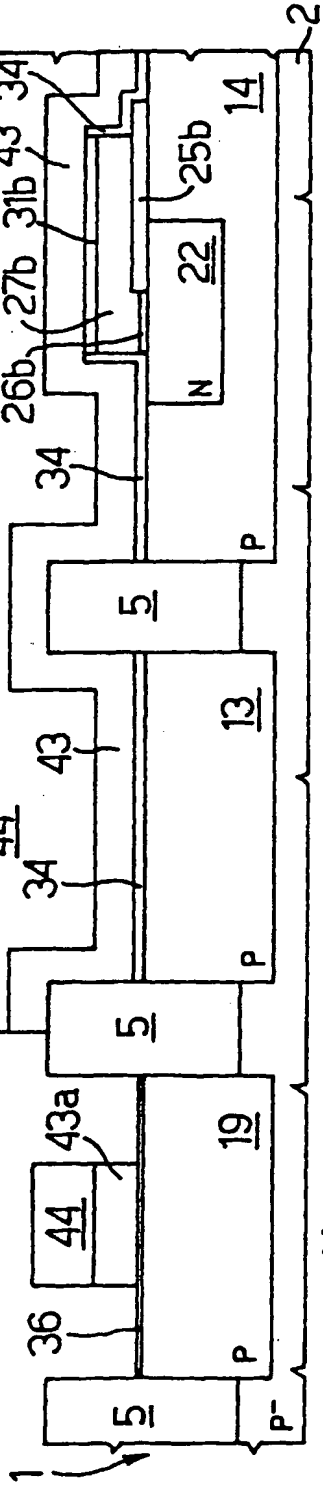


Fig.18

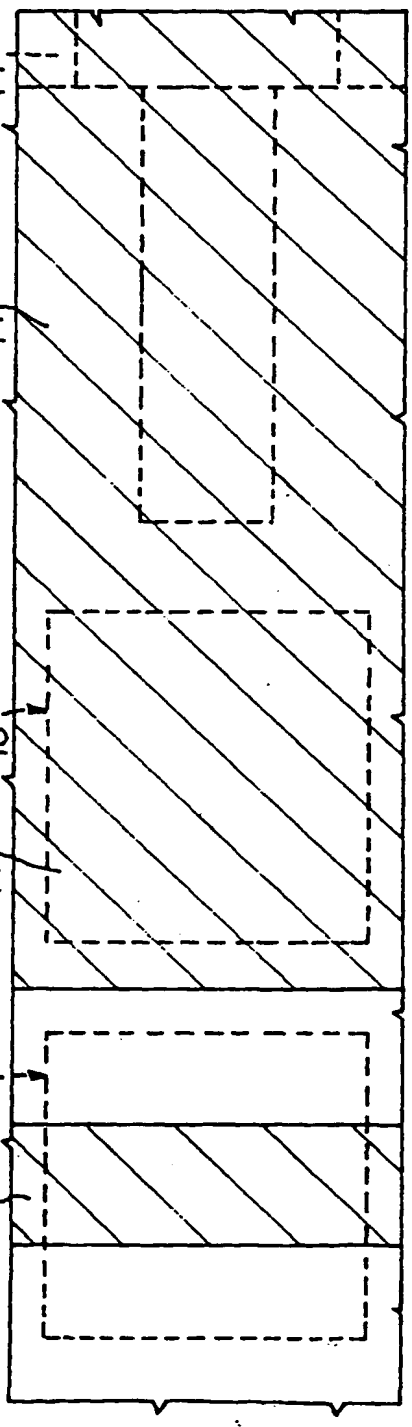
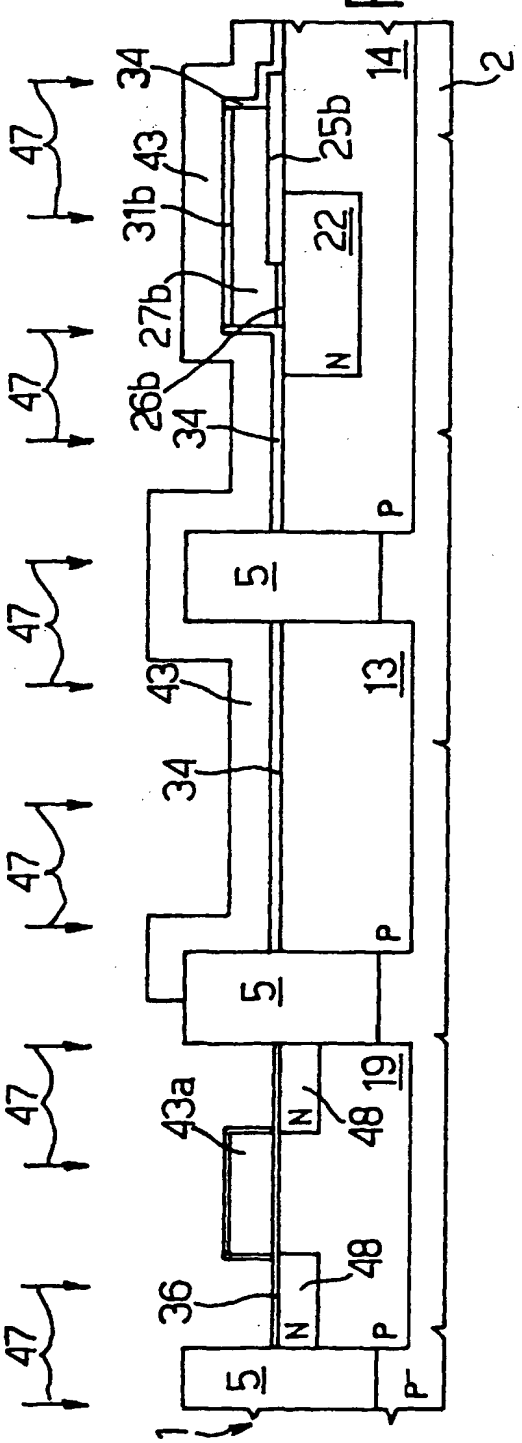


Fig.19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34
43
31b
27b
26b
25b
14
2
22
N
P
5
13
43a
48
19
36
1

Fig.20

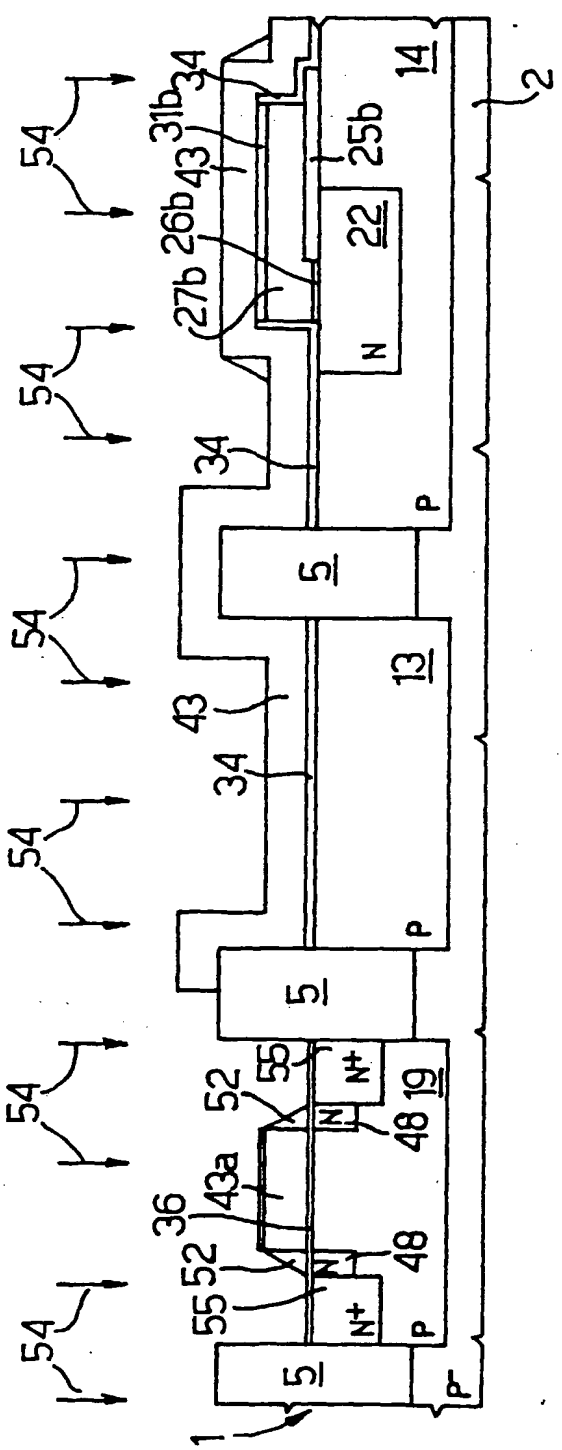
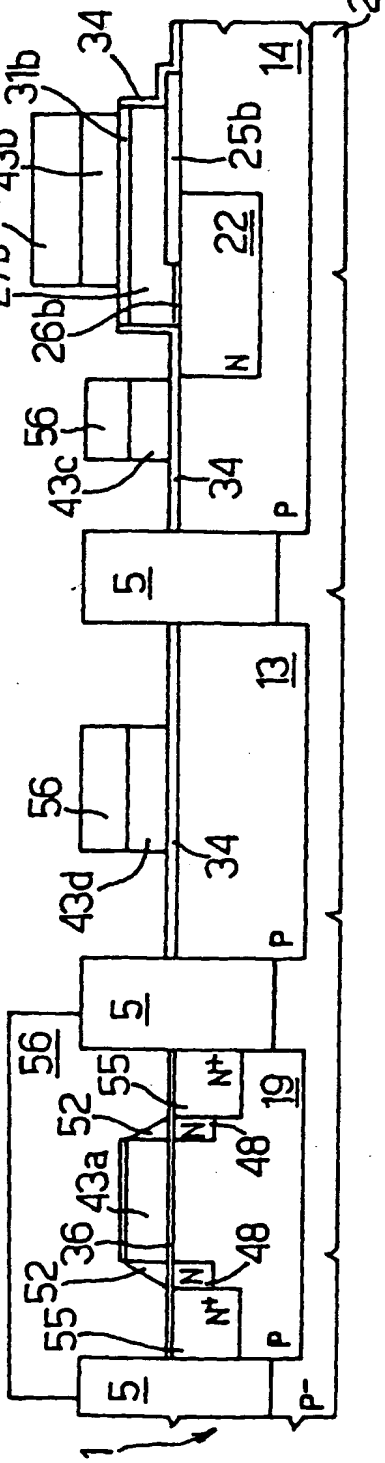

54
34
31b
43
26b
27b
25b
14
2
22
N
P
5
13
52
55
N+
48
19
43a
36
1

Fig.21


1
2
5
P-
P
N+
N
13
14
19
22
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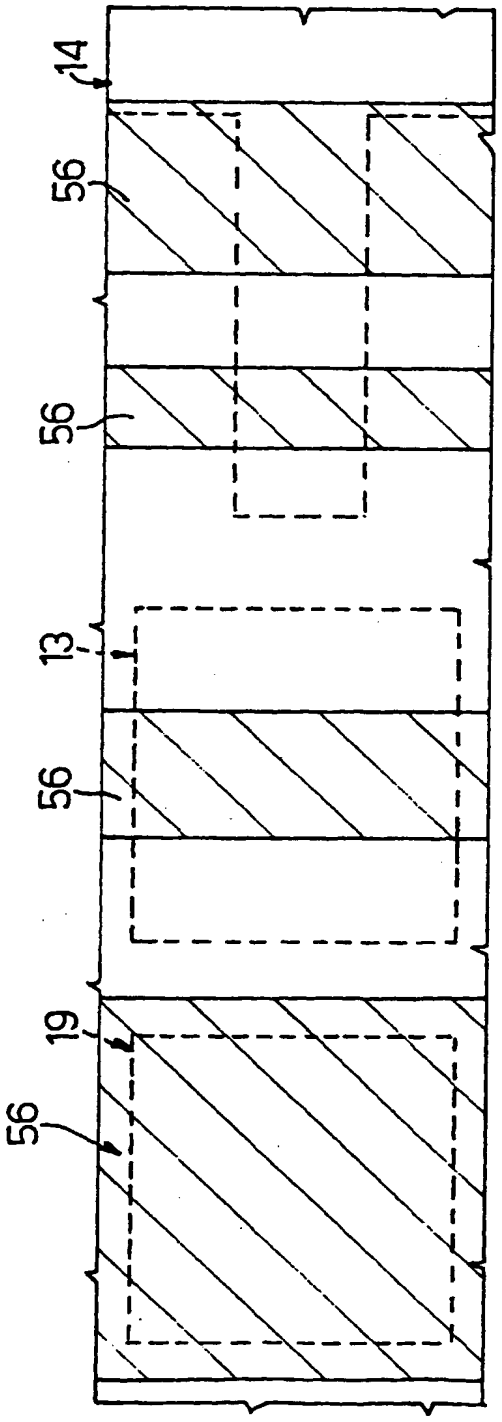
27b
31b
34
36
43a
43b
43c
43d
48
52
55
56

Fig.22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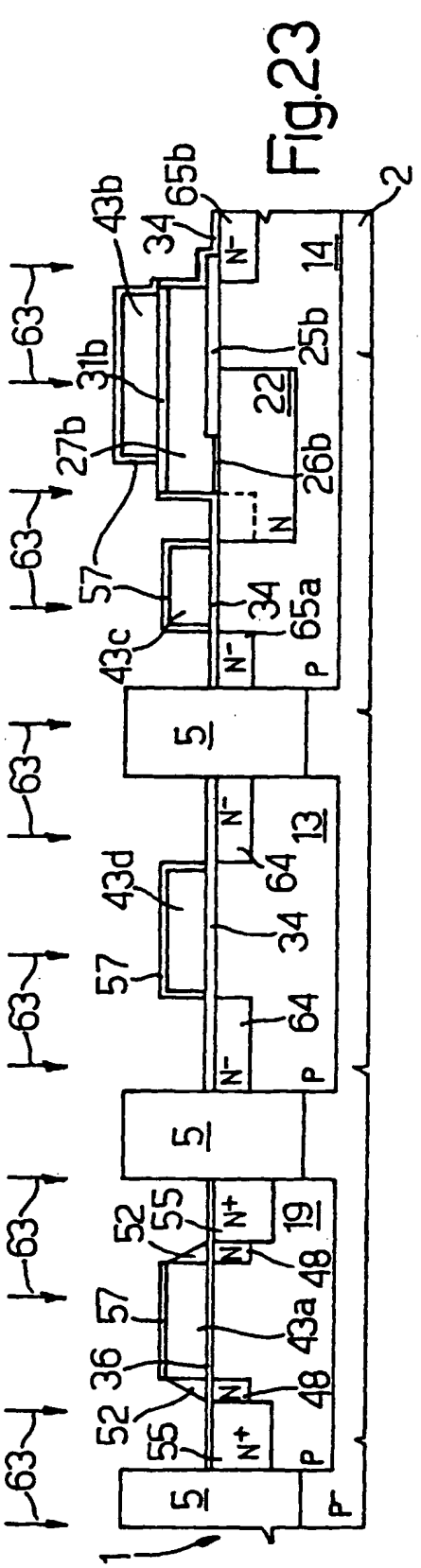
Fig.23
1
2
5
P-
P
N+
N
N-
13
14
19
22
34
36
43a
43b
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43d
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52
55
57
63
64
65a
65b
25b
26b
27b
31b

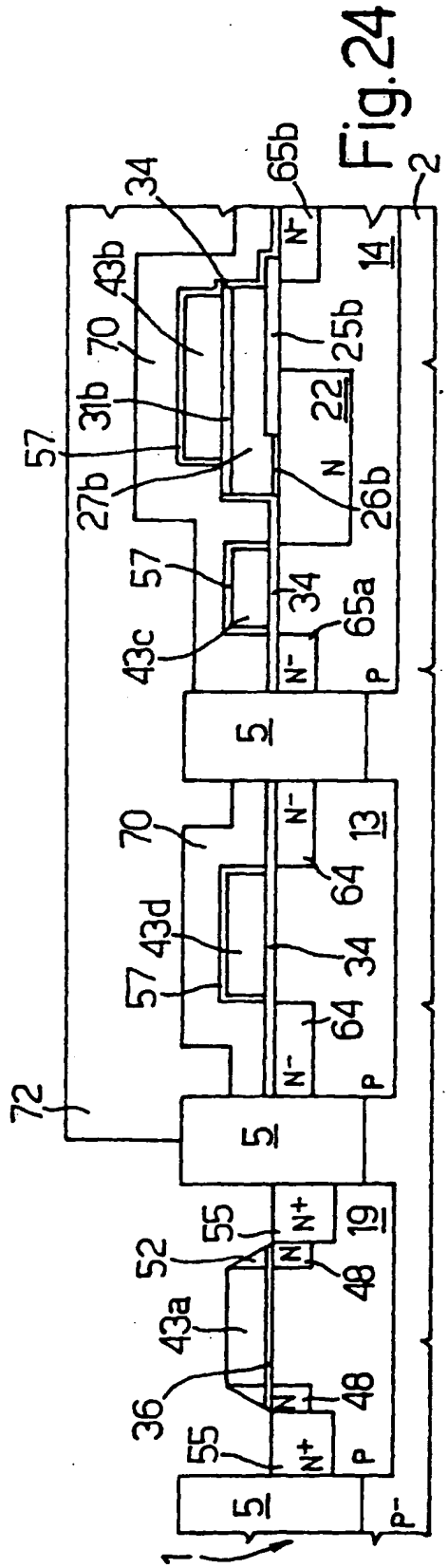
Fig.24
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2
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P-
P
N+
N
N-
13
14
19
22
34
36
43a
43b
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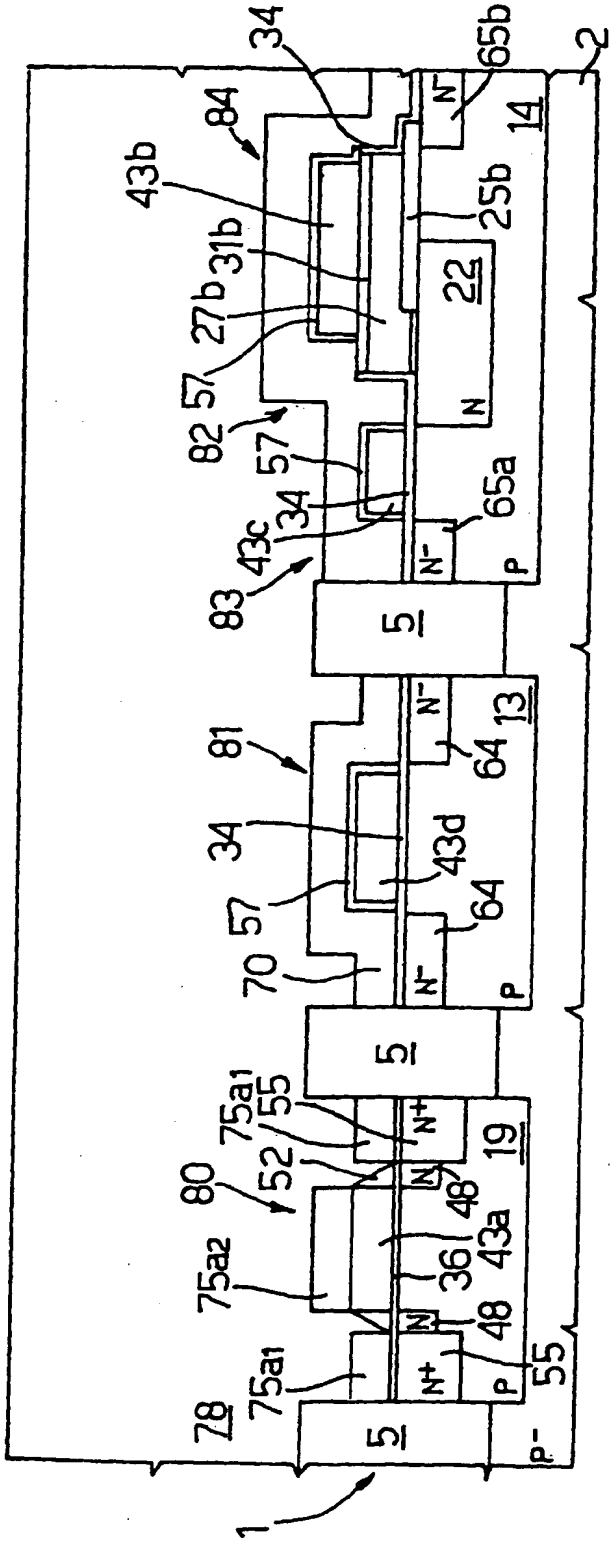
65a
65b
25b
26b
27b
31b
70
72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27b
57
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65a
34
43c
N-
P
83
5
81
N-
13
64
34
43d
57
64
70
N-
P
5
75a1
55
N+
19
80
52
N
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36
48
N
N+
P
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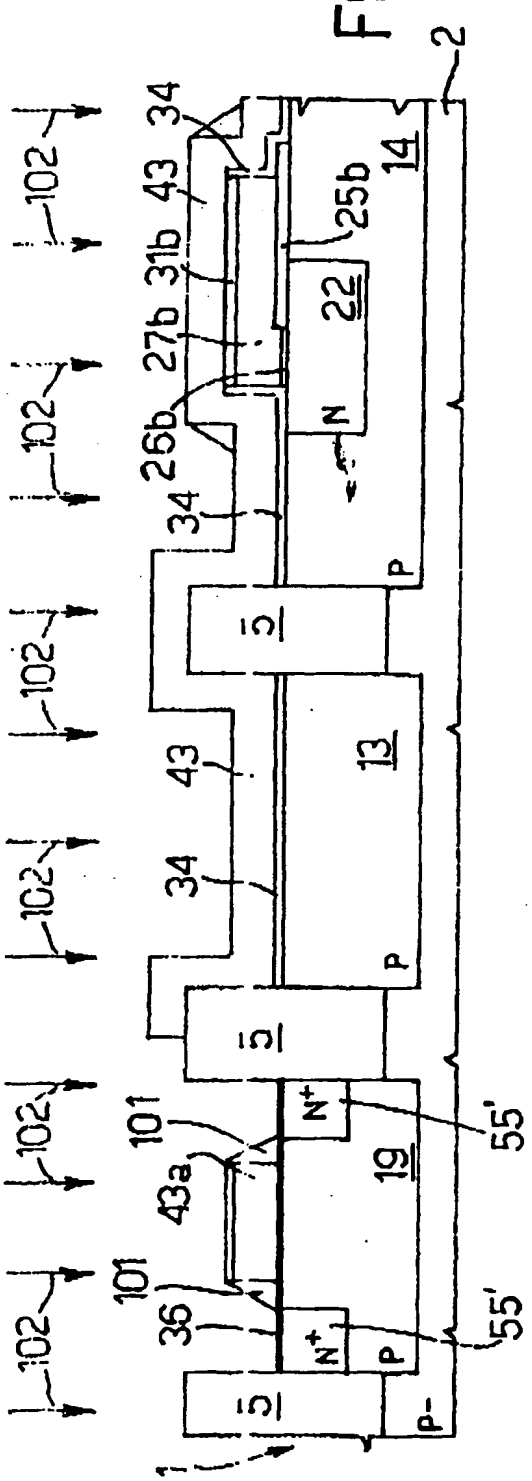
78
75a1
5
P-
1

Fig. 25

Fig.26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34
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25b
14
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27b
N
26b
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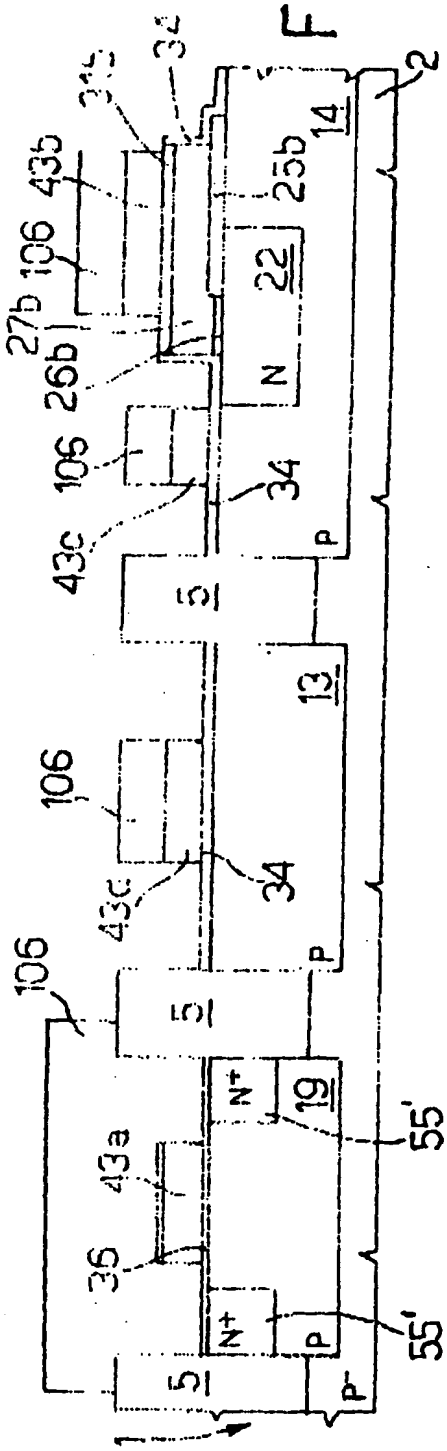
P
13
43
34
P
N+
55'
101
19
43a
101
36
N+
P
55'
P-
1
102
102
102
102
102
102
102

Fig.27


1
2
5
5
5
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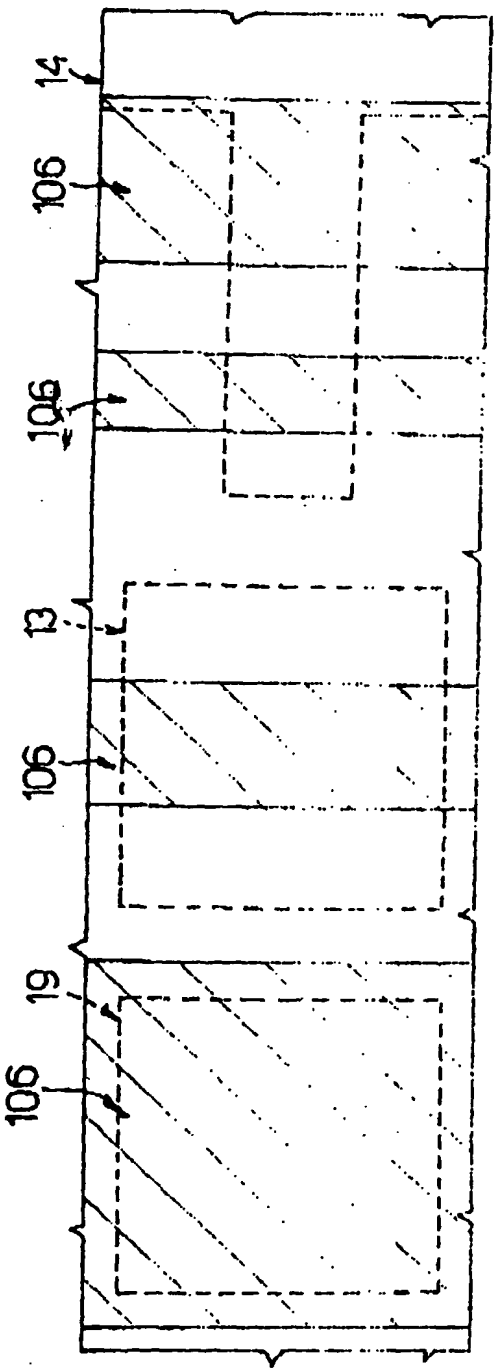
14
19
22
25b
26b
27b
34
34
34
35
43a
43b
43c
43c
55'
55'
106
106
106
106
106
106
106
N
N+
N+
P
P
P
P-

Fig.28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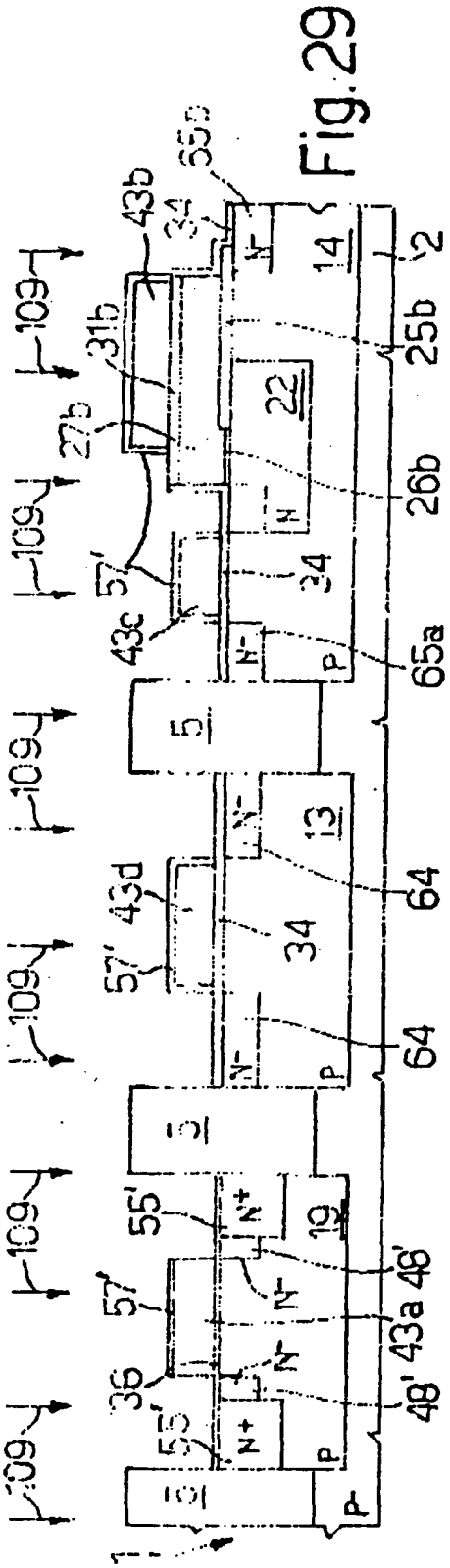

Fig.29

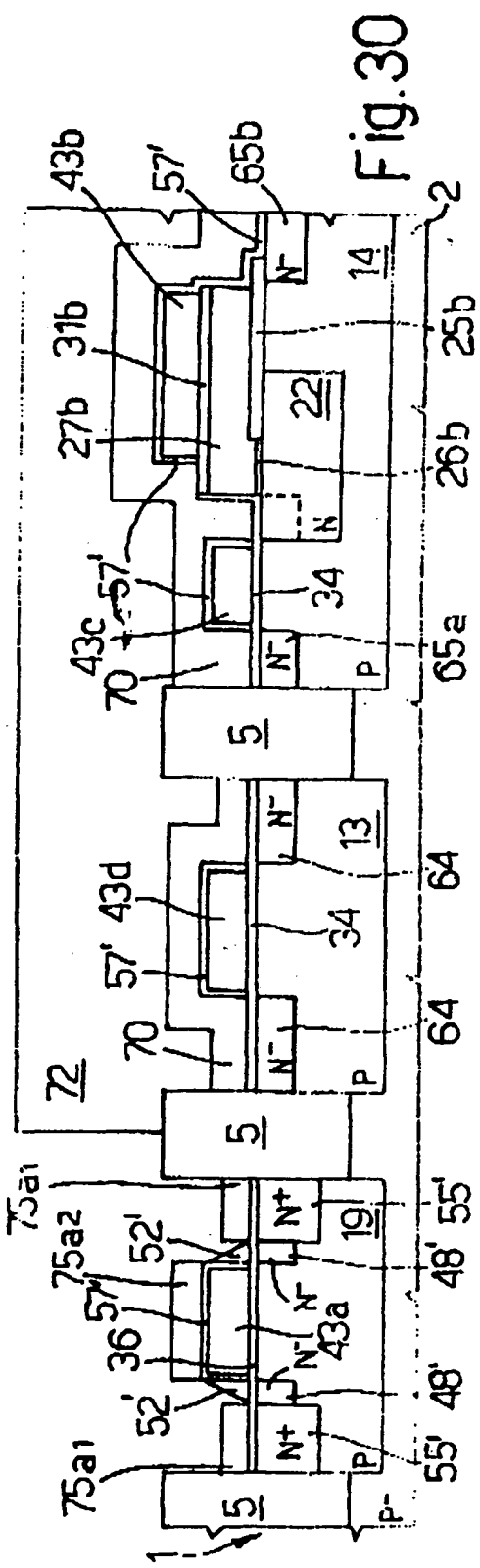

Fig.30

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 83 0771

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP 0 811 983 A (SGS THOMSON MICROELECTRONICS) 10 December 1997 * page 3, column 3, line 6 - page 4, column 6, line 38; figures 1-27 *	1,4,8,9	H01L21/8239 H01L27/105
A	EP 0 216 053 A (MOTOROLA INC) 1 April 1987 * page 3, column 4, line 38 - page 5, column 7, line 45; figures 1A-H *	1-3,5-7, 11	
A	PATENT ABSTRACTS OF JAPAN vol. 098, no. 002, 30 January 1998 -& JP 09 283643 A (ROHM CO LTD), 31 October 1997 * abstract *	1,4	
A	US 5 472 887 A (HUTTER LOUIS N ET AL) 5 December 1995 * column 12, line 52 - column 15, line 12; figures 21-29 *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	27 May 1999	Albrecht, C

CATEGORY OF CITED DOCUMENTS

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27-05-1999

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